based on a level shift input signal at the first power supply level. Consequently, as the potential difference between first and second power supplies increases, it becomes difficult to fully weaken the bond of the PMOS cross-coupled pair, and a level shift cannot be performed at a satisfactory speed.

It is therefore an object of the present invention to provide a level shift circuit capable of performing a level shift at a satisfactory speed while ensuring the margin of level shift operation when the potential difference between first and second power supplies increases.

DISCLOSURE OF THE INVENTION

In accordance with the present invention set forth in claim 1, a level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, includes a level shift core circuit which is controlled by a control circuit and/ or controls a pull-up and/ or pull-down circuit, wherein the level shift core circuit, being fed from the second power supply, receives signals output from the first logic circuit and outputs signals to be input to the second logic circuit.

In accordance with the present invention set forth in claim 2, a level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, comprises: a level shift core circuit for implementing a level shift; a pull-up and/ or pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and a control circuit fed from the second power supply which receives level shift input signals and the level shift output signals for controlling the pull-up and/ or pull-down circuit.

In accordance with the present invention set forth in claim 3, in the level shift circuit according to claim 1 or 2, the level shift core circuit

comprises a PMOS cross-coupled latch including a plurality of PMOSs and a differential NMOS switch including a plurality of NMOSs, wherein the source of each PMOS is connected to the second power supply, the gate of each PMOS is connected to the level shift output through the drain of another PMOS, the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is connected to the level shift input.

In accordance with the present invention set forth in claim 4, in the level shift circuit according to claim 2 or 3, the control circuit comprises: a NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; a NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NAND circuits, respectively, wherein the respective NAND circuits and inverters output a signal as a control signal.

In accordance with the present invention set forth in claim 5, in the level shift circuit according to claim 4, the NAND circuit has CMOS circuitry, and each PMOS connected to the level shift input is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

In accordance with the present invention set forth in claim 6, in the level shift circuit according to one of claims 1 to 5, the pull-up and/ or pull-down circuit comprises: a plurality of PMOSs each having a source connected to the second power supply, a gate connected to the control signal from the control circuit, and a drain connected to the level shift output; and a plurality of NMOSs each having a source connected to the ground voltage

GND, a gate connected to the control signal from the control circuit, and a drain connected to the level shift output.

In accordance with the present invention set forth in claim 7, in the level shift circuit according to one of claims 1 to 3, the control circuit comprises: a NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; a NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and a plurality of inverters fed from the second power supply, which receives the outputs of the NOR circuits, respectively, wherein the respective NOR circuits and inverters output a signal as a control signal.

In accordance with the present invention set forth in claim 8, in the level shift circuit according to claim 7, the NOR circuit has CMOS circuitry, and each PMOS connected to the level shift input is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

In accordance with the present invention set forth in claim 9, in the level shift circuit according to one of claims 1 to 8, the level shift core circuit comprises: a PMOS cross-coupled latch including a plurality of PMOSs each having a source connected to the second power supply and a gate connected to the level shift output; a plurality of PMOS switches each having a source connected to the drain of one of the PMOSs, a gate connected to the level shift input and a drain connected to the level shift output; and a differential NMOS switch including a plurality of NMOSs each having a source connected to the ground voltage GND, a drain connected to the level shift output and a gate connected to the level shift input.

In accordance with the present invention set forth in claim 10, in the

level shift circuit according to one of claims 1 to 9, the level shift core circuit comprises: a PMOS cross-coupled latch including a plurality of PMOSs each having a source connected to the second power supply and a gate connected to the level shift output through the drain of another PMOS; a differential NMOS switch including a plurality of NMOSs each having a source connected to the ground voltage GND, a drain connected to the level shift output and a gate connected to the level shift input; and NMOSs each having a drain connected to the first power supply, a gate connected to the level shift input and a source connected to the level shift output.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing an example of a conventional level shift circuit.

Fig. 2 is a circuit diagram showing another example of a conventional level shift circuit.

Fig. 3 is a circuit diagram showing yet another example of a conventional level shift circuit.

Fig. 4 is a circuit diagram showing another example of a control circuit according to a modified example of the second embodiment of the present invention.

Fig. 5 is a circuit diagram showing yet another example of a control circuit according to a modified example of the second embodiment of the present invention.

Fig. 6 is a circuit diagram showing another example of a control circuit according to the second embodiment of the present invention.

Fig. 7 is a diagram showing a level shift circuit according to an embodiment of the present invention.

Fig. 8 is a diagram showing an example of a level shift core circuit used for a level shift circuit of the present invention.

Fig. 9 is a diagram showing an example of a control circuit used for a

CLAIMS

1. A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, including a level shift core circuit which is controlled by a control circuit and/ or controls a pull-up and/ or pull-down circuit, wherein the level shift core circuit, being fed from the second power supply, receives signals output from the first logic circuit and outputs signals to be input to the second logic circuit.

2. A level shift circuit for changing the signal level in a first logic circuit fed from a first power supply to the signal level in a second logic circuit fed from a second power supply, the level shift circuit comprising:

a level shift core circuit for implementing a level shift;

a pull-up and/ or pull-down circuit fed from the second power supply for pulling up and/ or pulling down level shift output signals from the level shift core circuit; and

a control circuit fed from the second power supply, which receives level shift input signals and the level shift output signals for controlling the pull-up and/ or pull-down circuit.

3. The level shift circuit claimed in claim 1 or 2, wherein the level shift core circuit comprises a PMOS cross-coupled latch including a plurality of PMOSs and a differential NMOS switch including a plurality of NMOSs:

wherein the source of each PMOS is connected to the second power supply, the gate of each PMOS is connected to the level shift output through the drain of another PMOS, the source of each NMOS of the differential NMOS switch is connected to the ground voltage GND, the drain of each NMOS is connected to the level shift output, and the gate of each NMOS is

connected to the level shift input.

4. The level shift circuit claimed in claim 2 or 3, wherein the control circuit comprises:

a NAND circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals;

a NAND circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals; and

a plurality of inverters fed from the second power supply, which receives the outputs of the NAND circuits, respectively;

wherein the respective NAND circuits and inverters output a signal as a control signal.

5. The level shift circuit claimed in claim 4, wherein the NAND circuit has CMOS circuitry, and each PMOS connected to the level shift input is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

6. The level shift circuit claimed in one of claims 1 to 5, wherein the pull-up and/ or pull-down circuit comprises: a plurality of PMOSs each having a source connected to the second power supply, a gate connected to the control signal from the control circuit, and a drain connected to the level shift output; and a plurality of NMOSs each having a source connected to the ground voltage GND, a gate connected to the control signal from the control circuit, and a drain connected to the level shift output.

7. The level shift circuit claimed in one of claims 1 to 3, wherein the control circuit comprises:

a NOR circuit fed from the second power supply, which receives an inverted signal of the level shift input signals and a non-inverted signal of the level shift output signals;

a NOR circuit fed from the second power supply, which receives a non-inverted signal of the level shift input signals and an inverted signal of the level shift output signals; and

a plurality of inverters fed from the second power supply, which receives the outputs of the NOR circuits, respectively, wherein:

the respective NOR circuits and inverters output a signal as a control signal.

8. The level shift circuit claimed in claim 7, wherein the NOR circuit has CMOS circuitry, and each PMOS connected to the level shift input is a transistor which satisfies at least one of the conditions that the channel width/ channel length ratio is low or that the polarity of the threshold voltage is negative and the absolute value of the threshold voltage is large.

9. The level shift circuit claimed in one of claims 1 to 8, wherein the level shift core circuit comprises:

a PMOS cross-coupled latch including a plurality of PMOSs each having a source connected to the second power supply and a gate connected to the level shift output;

a plurality of PMOS switches each having a source connected to the drain of one of the PMOSs, a gate connected to the level shift input and a drain connected to the level shift output; and

a differential NMOS switch including a plurality of NMOSs each having a source connected to the ground voltage GND, a drain connected to

the level shift output and a gate connected to the level shift input.

10. The level shift circuit claimed in one of claims 1 to 9, wherein the level shift core circuit comprises:

a PMOS cross-coupled latch including a plurality of PMOSs each having a source connected to the second power supply and a gate connected to the level shift output through the drain of another PMOS;

a differential NMOS switch including a plurality of NMOSs each having a source connected to the ground voltage GND, a drain connected to the level shift output and a gate connected to the level shift input; and

NMOSs each having a drain connected to the first power supply, a gate connected to the level shift input and a source connected to the level shift output.